

We claim:

1. A RRAM memory cell formed on a silicon substrate having a operative junction therein and a metal plug formed thereon, comprising:

a first oxidation resistive layer;

5 a first refractory metal layer;

a CMR layer;

a second refractory metal layer; and

a second oxidation resistive layer.

10 2. The RRAM memory cell of claim 1 wherein the oxidation resistive layers are formed of a material taken from the group of materials consisting of TiN, TaN, TiAlN<sub>x</sub>, TaAlN<sub>x</sub>, TaSiN, TiSiN, and RuTiN.

15 3. The RRAM memory cell of claim 2 wherein the oxidation resistive layers have a thickness of between about 50 nm to 300 nm.

4. The RRAM memory cell of claim 1 wherein the refractory metal layers are formed of a material taken from the group of materials consisting of Pt, Ir, IrO<sub>2</sub>, Ru, RuO<sub>2</sub>, Au, Ag, Rh, Pd, Ni, and Co.

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5. The RRAM memory cell of claim 4 wherein the refractory metal layers have a thickness of between about 3 nm to 50 nm.

6. The RRAM memory cell of claim 1 wherein the CMR layer is formed of a material  
5 taken from the group of material consisting of CMR materials and high-temperature superconductors.

7. The RRAM memory cell of claim 6 wherein the CMR layer has a thickness of between about 50 nm to 300 nm.

8. A method of fabricating a multi-layer electrode RRAM memory cell comprising:  
preparing a silicon substrate;  
forming a junction in the substrate taken from the group of junctions consisting of  
N+ junctions and P+ junctions;

5 depositing a metal plug on the junction;  
depositing a first oxidation resistant layer on the metal plug;  
depositing a first refractory metal layer on the first oxidation resistant layer;  
depositing a CMR layer on the first refractory metal layer;  
depositing a second refractory metal layer on the CMR layer;  
10 depositing a second oxidation resistant layer on the second refractory metal layer;  
and  
completing the RRAM memory cell.

9. The method of claim 8 wherein said depositing the oxidation resistive layers  
15 includes depositing a material taken from the group of materials consisting of TiN, TaN, TiAlN<sub>x</sub>,  
TaAlN<sub>x</sub>, TaSiN, TiSiN, and RuTiN.

10. The method of claim 9 wherein said depositing the oxidation resistive layers  
includes depositing the oxidation resistive layers to a thickness of between about 50 nm to 300 nm.

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11. The method of claim 8 wherein said depositing the refractory metal layers includes depositing a material taken from the group of materials consisting of Pt, Ir, IrO<sub>2</sub>, Ru, RuO<sub>2</sub>, Au, Ag, Rh, Pd, Ni, and Co.

5 12. The method of claim 11 wherein said depositing the refractory metal layers includes depositing the refractory metal to a thickness of between about 3 nm to 50 nm.

13. The method of claim 8 wherein said depositing a CMR layer includes depositing a layer of CMR material taken from the group of material consisting of PCMO, LPCMO and high-  
10 temperature superconductors.

14. The method of 13 wherein said depositing a CMR layer includes depositing a layer of CMR material having a thickness of between about 50 nm to 300 nm.